LISTING OF CLAIMS

1. (Previously Presented) A semiconductor device comprising a semiconductor body which is provided with a field effect transistor at a surface and which comprises strongly doped source and drain zones and a channel region extending between the source zone and the drain zone, with a gate electrode being present which overlaps the channel region upon perpendicular projection thereon, wherein the source zone, the drain zone and the gate electrode are connected at the surface to a metal source contact, a drain contact and a gate electrode contact, respectively in the form of metal strips, and wherein a further metal strip is positioned between the gate electrode contact and the drain contact, which further metal strip is insulated from the semiconductor body, is locally electrically connected to the metal source contact, and forms a shield between the gate electrode and the drain contact, characterized in that the electrical connection between the further metal strip and the metal source contact comprises a capacitor, and in that the further metal strip is provided with a connecting contact for applying an external voltage to the further metal strip.

2. (Previously Presented) The semiconductor device as claimed in claim 1, characterized in that the capacitor is integrated in the semiconductor body and is positioned within the active region beside the transistor.

3. (Previously Presented) The semiconductor device as claimed in claim 2, characterized in that the source contact, the drain contact, the gate electrode contact, an electrode of the capacitor and the connecting contact thereof, are formed in a first metal layer, and the further metal strip is formed in a second metal layer arranged below the first metal layer, and wherein the first and second layers are separated from one another by a further insulating layer.

4. (Previously Presented) The semiconductor device as claimed in claim 3, characterized in that the other electrode of the capacitor is formed by the semiconductor body, which comprises a strongly doped substrate on which a more weakly doped epitaxial layer is present.

5. (Previously Presented) The semiconductor device as claimed in claim 3, characterized in that the two electrodes of the capacitor form part of the metal layers, and the lower electrode of said two electrodes is electrically connected to the semiconductor body, which comprises a strongly doped region at that location.

6. (Previously Presented) The semiconductor device as claimed in claim 1, characterized in that the capacitance value of the capacitor ranges between 10 pF and 1 nF at an operating frequency ranging between 100 MHz and 3 GHz.

7. (Previously Presented) The semiconductor device as claimed in claim 1, characterized in that the field effect transistor is a MOS transistor, in which the semiconductor body comprises a comparatively weakly doped region of a first conductivity type adjoining the surface, which region is provided with the strongly doped source and drain zone of the opposed, second conductivity type and a weakly doped drain extension between the drain zone and the channel region, wherein the gate electrode is electrically insulated from the channel region and an electrically insulating layer is laid over the surface, which layer is provided with contact windows above the source zone, the drain zone and the gate electrode, through which contact windows the source zone, the drain zone and the gate electrode, respectively, are connected to the contacts.

8. (Previously Presented) The semiconductor device as claimed in claim 1, characterized in that the metal strips serving as the contacts of the source zone, the drain zone and the gate electrode are embodied as parallel metal strips positioned beside each other.

9. (Previously Presented) The semiconductor device as claimed in claim 1, characterized in that another metal strip is present between the further metal strip and the gate electrode, which other strip is separated from the semiconductor body by an electrically insulating layer and may or may not be provided with another connecting contact for applying another external voltage.

10. (Previously Presented) A method of operating a semiconductor device as claimed in claim 1, wherein a voltage is applied to the contact region of the further metal strip during operation of the device.

11. (Previously Presented) The method as claimed in claim 10, characterized in that the applied voltage is selected independent of the power range within which the device operates.